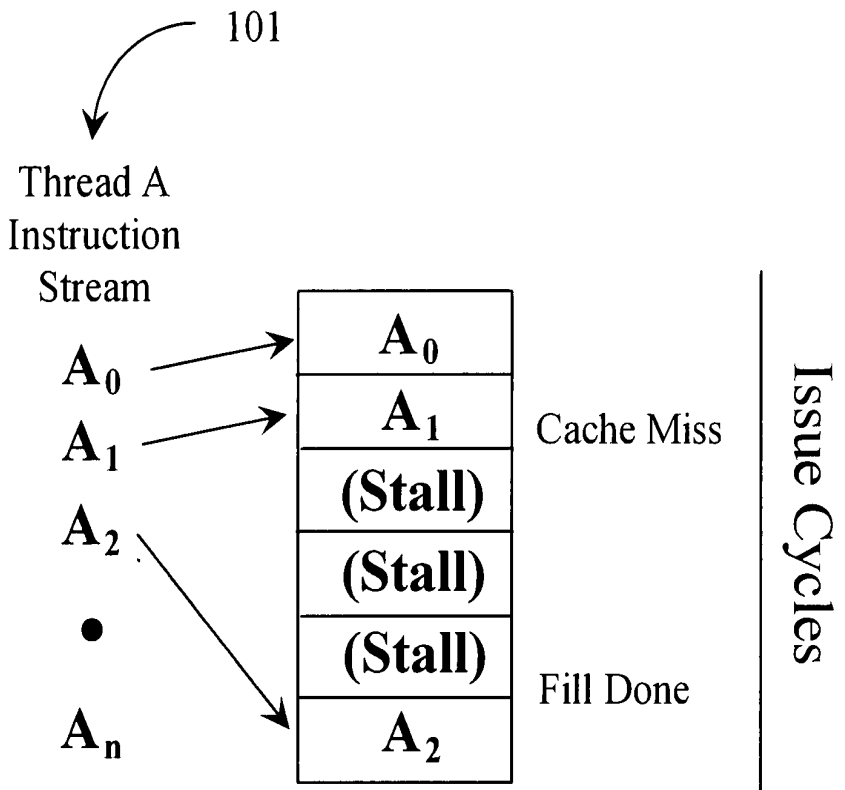

101
Thread A
Instruction
Stream
A0
A1
A2
An
A0
A1
(Stall)
(Stall)
(Stall)
A2
Cache Miss
Fill Done
Issue Cycles

Fig. 1A

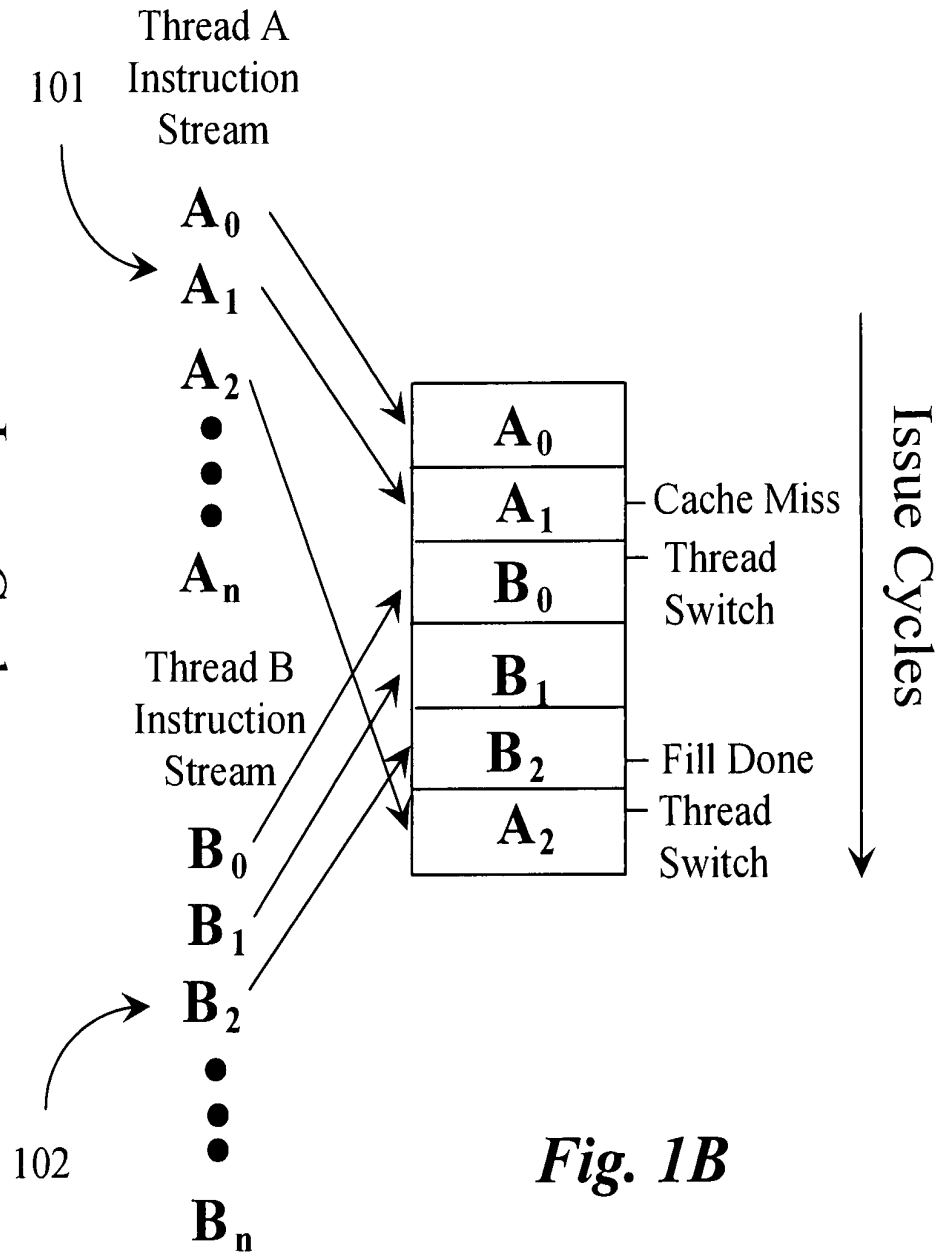

101
Thread A
Instruction
Stream
A0
A1
A2
An
Thread B
Instruction
Stream
B0
B1
B2
Bn
102
A0
A1
B0
B1
B2
A2
Cache Miss
Thread
Switch
Fill Done
Thread
Switch
Issue Cycles

Fig. 1B

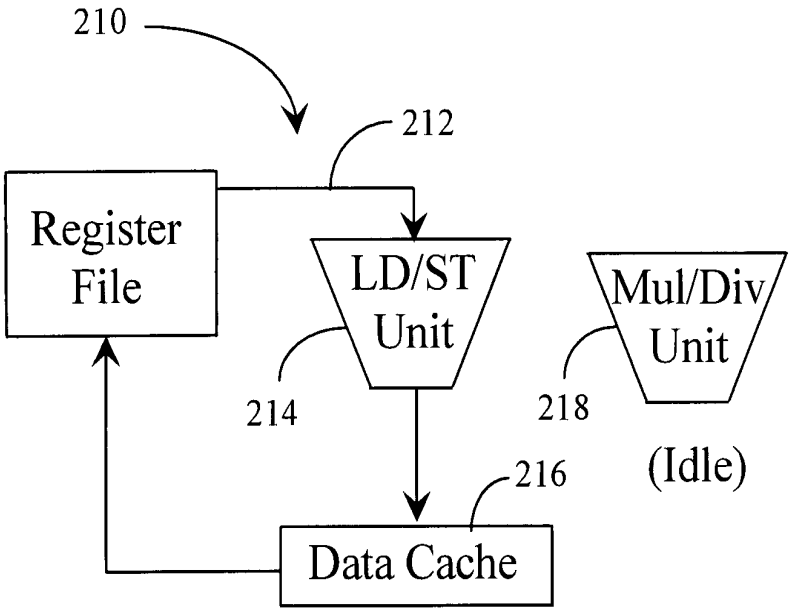

210
212
Register File
LD/ST Unit
Mul/Div Unit
214
218
(Idle)
216
Data Cache

Fig. 2A

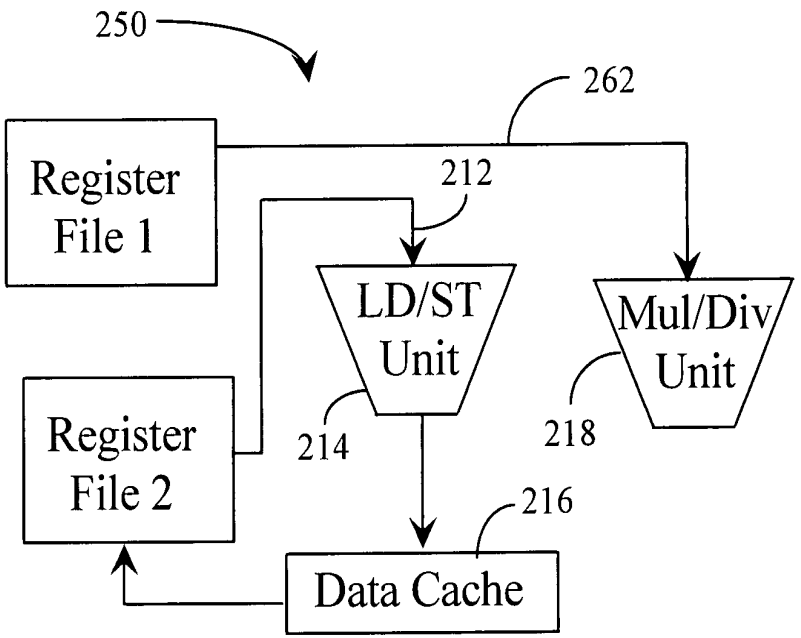

250
262
Register File 1
212
LD/ST Unit
Mul/Div Unit
Register File 2
214
218
216
Data Cache

Fig. 2B

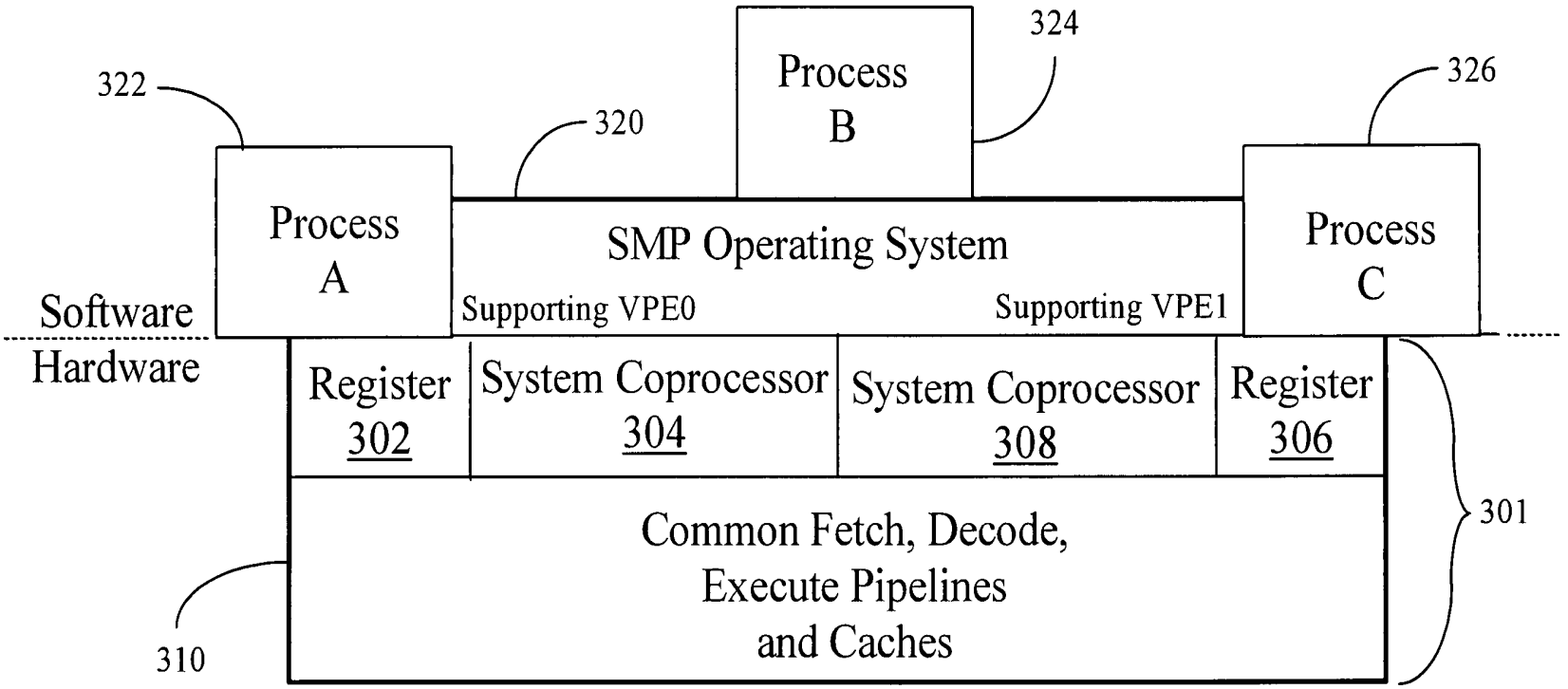

322
320
Process
B
324
326
Process
A
SMP Operating System
Supporting VPE0
Supporting VPE1
Process
C
Software
Hardware
Register
302
System Coprocessor
304
System Coprocessor
308
Register
306
301
Common Fetch, Decode,
Execute Pipelines
and Caches
310

Fig. 3

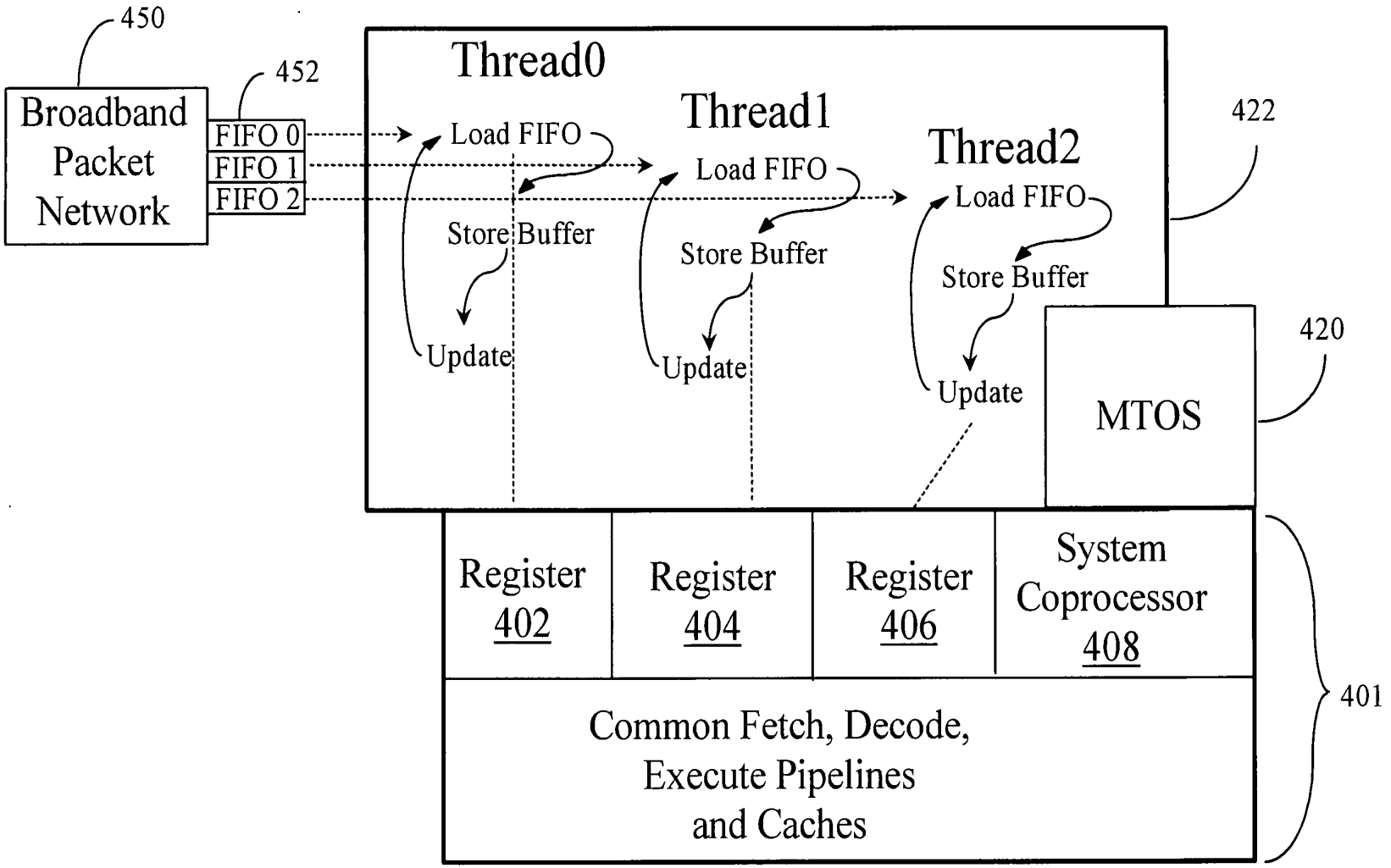

450
Broadband Packet Network
452
FIFO 0
FIFO 1
FIFO 2
Thread0
Thread1
Thread2
422
Load FIFO
Load FIFO
Load FIFO
Store Buffer
Store Buffer
Store Buffer
Update
Update
Update
420
MTOS
Register 402
Register 404
Register 406
System Coprocessor 408
Common Fetch, Decode, Execute Pipelines and Caches
401

Fig. 4

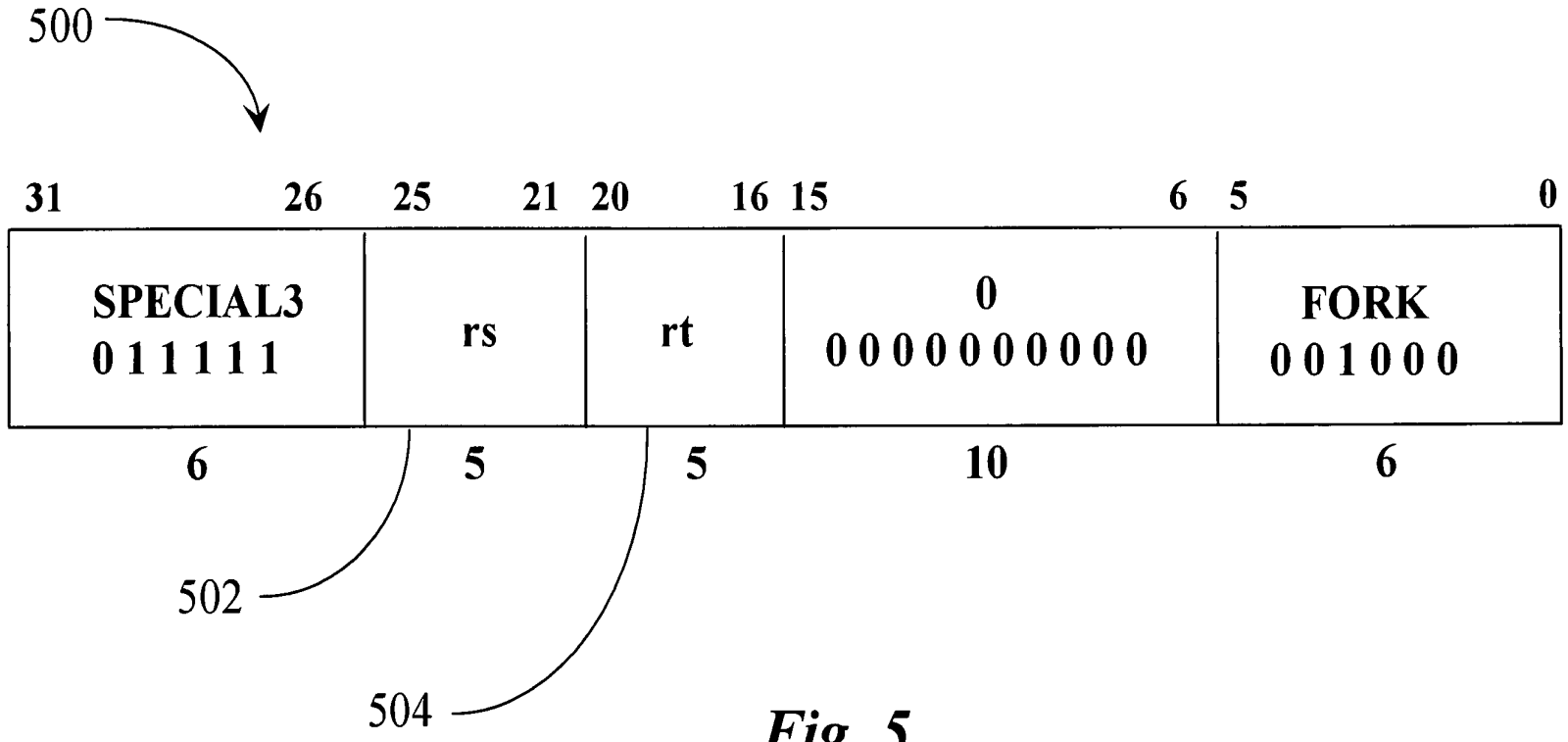

500
31
26
25
21
20
16
15
6
5
0
SPECIAL3
0 1 1 1 1 1
rs
rt
0
0 0 0 0 0 0 0 0 0 0
FORK
0 0 1 0 0 0
6
5
5
10
6
502
504

Fig. 5

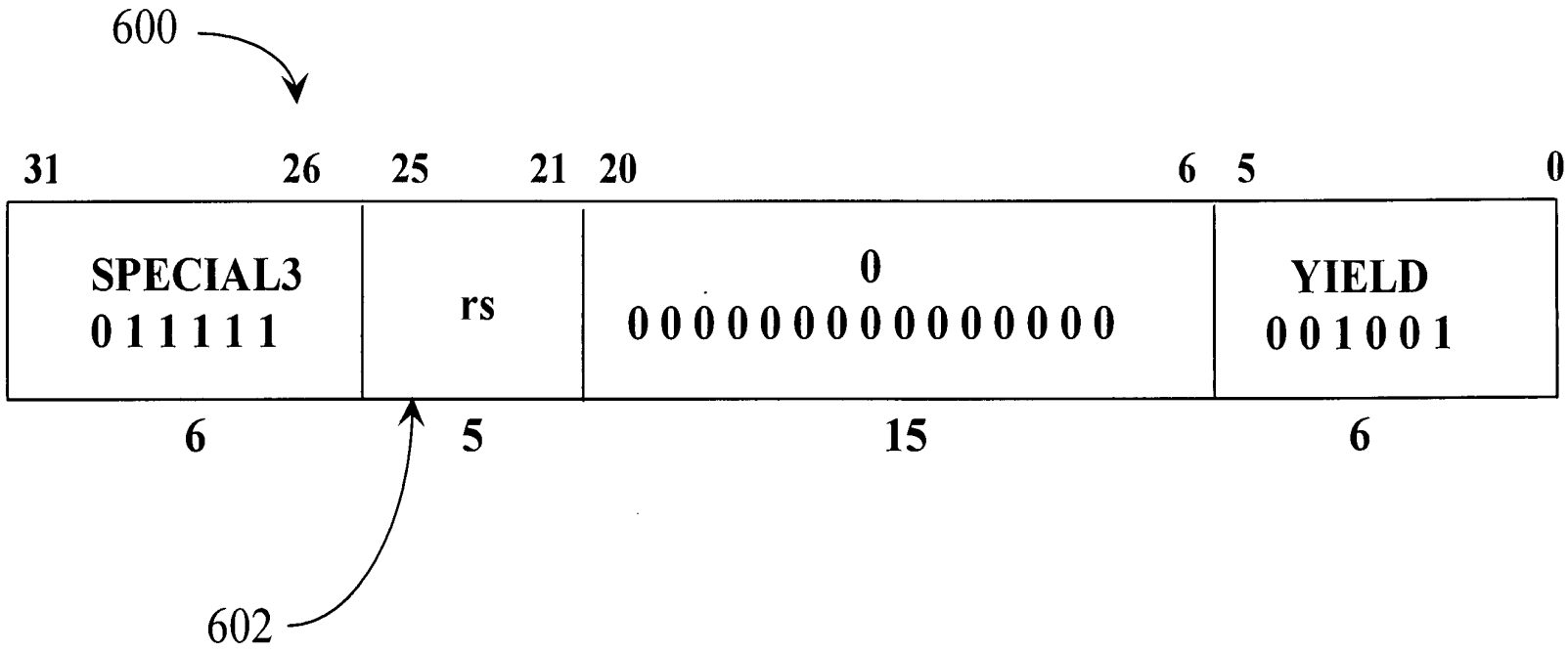
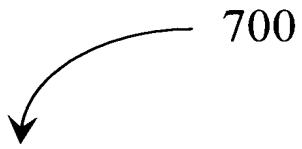

600
31
26
25
21
20
6
5
0
SPECIAL3
011111
rs
0
00000000000000000
YIELD
001001
6
5
15
6
602

Fig. 6



Contents of GPR rs	Thread Scheduling Enable Condition
MSB:16	Reserved. UNPREDICTABLE behavior if non-zero
15	IP7 Interrupt Asserted
14	IP6 Interrupt Asserted
13	IP5 Interrupt Asserted
12	IP4 Interrupt Asserted
11	IP3 Interrupt Asserted
10	IP2 Interrupt Asserted
9	IP1 Interrupt Asserted
8	IP0 Interrupt Asserted
7	Load-Linked Condition Clear
6	Load-Linked Condition Set
5	System Dependent External Event 3
4	System Dependent External Event 2
3	System Dependent External Event 1
2	System Dependent External Event 0
1	Reserved. UNPREDICTABLE behavior if non-zero
0	Enabled on Next Cycle

Fig. 7

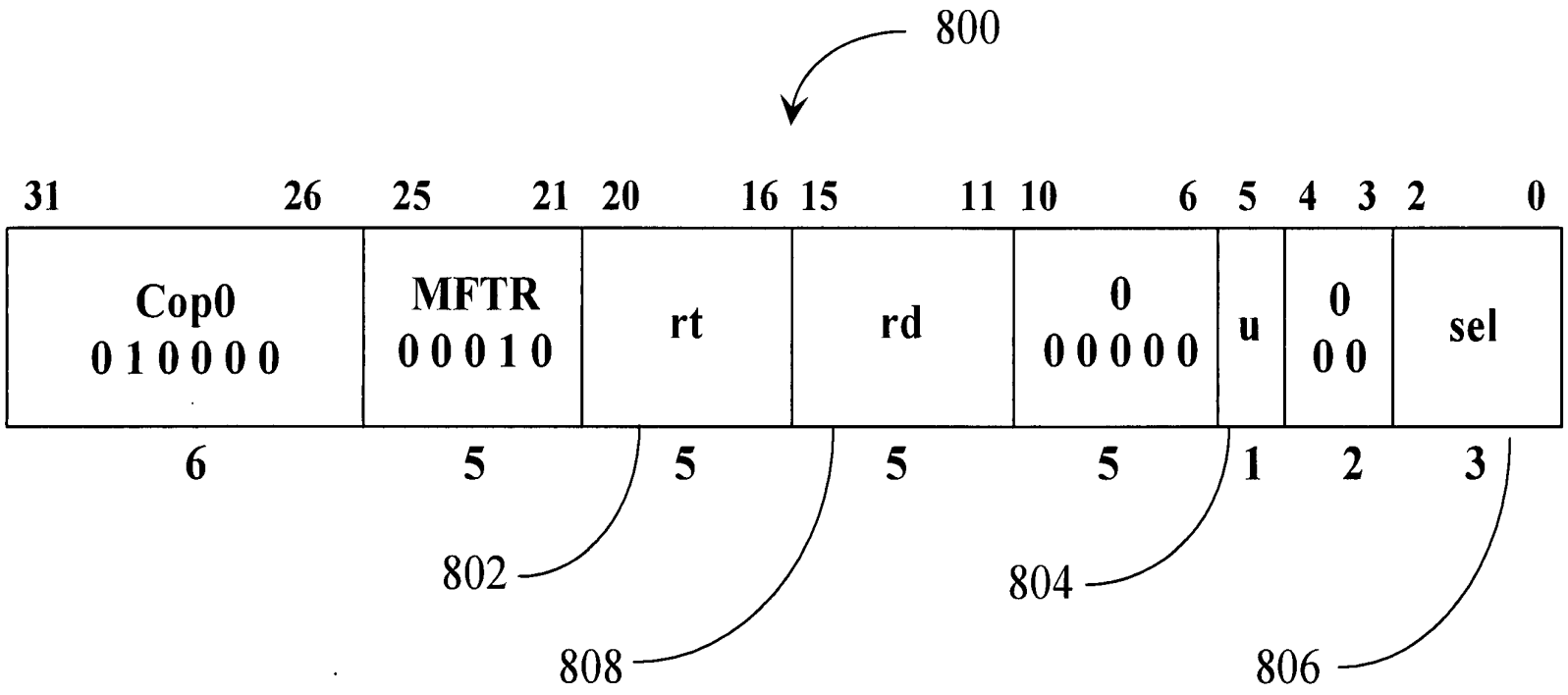

800
31
26
25
21
20
16
15
11
10
6
5
4
3
2
0
Cop0
0 1 0 0 0 0
MFTR
0 0 0 1 0
rt
rd
0
0 0 0 0 0
u
0
0 0
sel
6
5
5
5
5
1
2
3
802
808
804
806

Fig. 8

900

u value	sel value	Register Selected
0	n	Coprocessor 0 Register number rt, sel = sel
1	0	GPR[rt]
1	1	If rt = 0, Lo Register If rt = 1, Hi Register If rt = 2, ACX Register Other Values of rt, Reserved, Unpredictable
1	2	FPR[rt]
1	3	FPCR[rt]
1	4	Cop2 Data[rt]
1	5	Cop2 Control [rt]
1	>5	Reserved, Unpredictable

Fig. 9

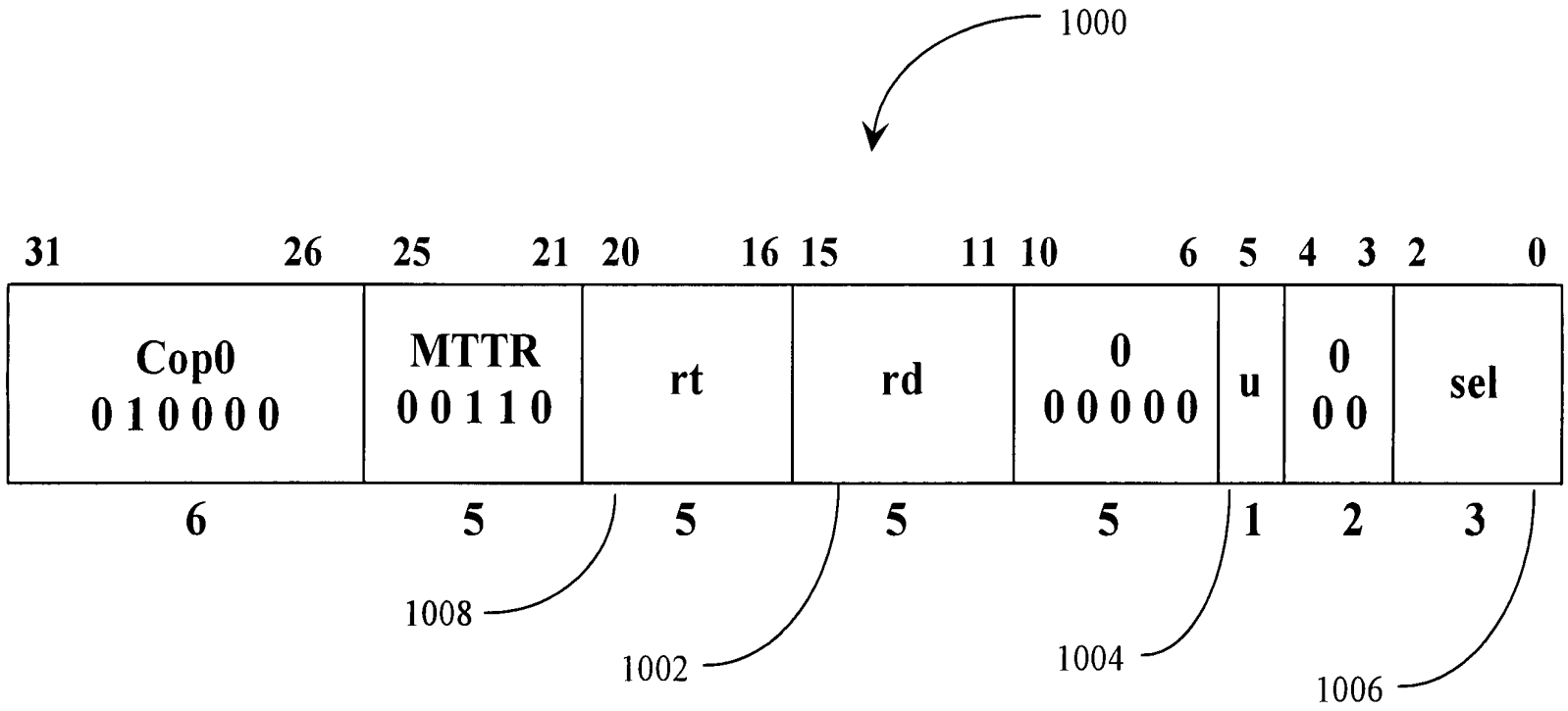
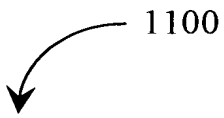

1000
31
26
25
21
20
16
15
11
10
6
5
4
3
2
0
Cop0
0 1 0 0 0 0
MTTR
0 0 1 1 0
rt
rd
0
0 0 0 0 0
u
0
0 0
sel
6
5
5
5
5
1
2
3
1008
1002
1004
1006

Fig. 10



u value	sel value	Register Selected
0	n	Coprocessor 0 Register number rd, sel = sel
1	0	GPR[rd]
1	1	If rd = 0, Lo Register If rd = 1, Hi Register If rd = 2, ACX Register Other Values of rd, Reserved, Unpredictable
1	2	FPR[rd]
1	3	FPCR[rd]
1	4	Cop2 Data[rd]
1	5	Cop2 Control [rd]
1	>5	Reserved, Unpredictable

Fig. 11

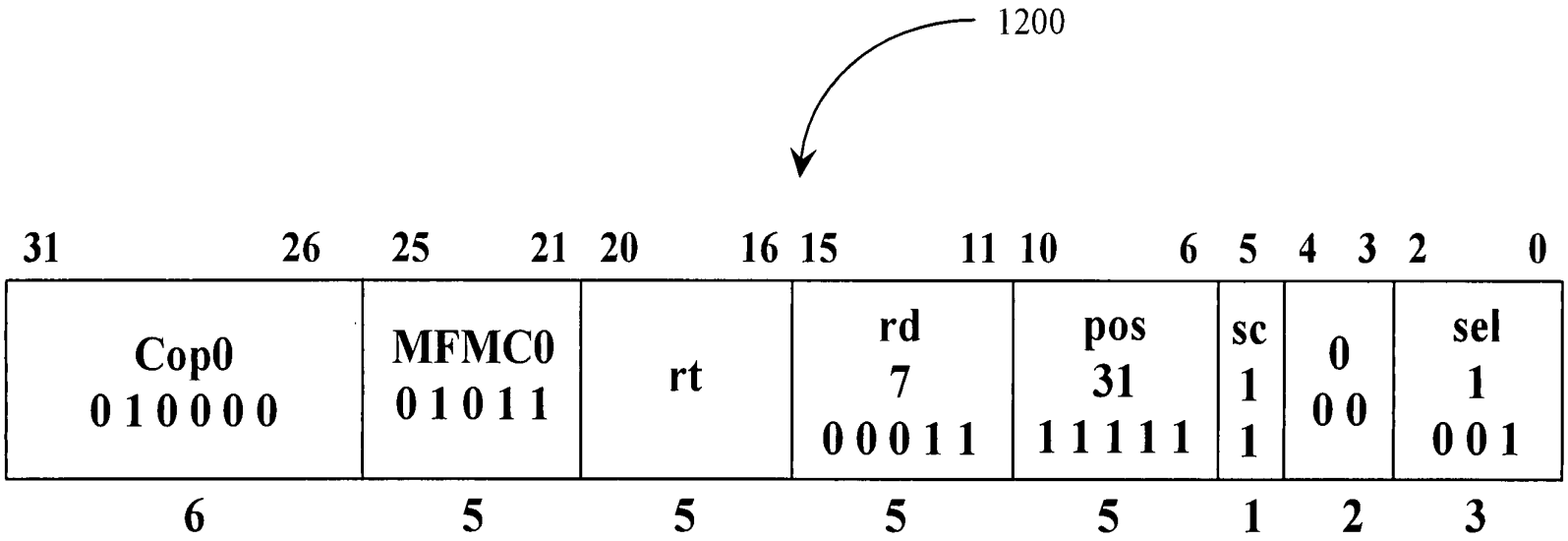

1200
31 26 25 21 20 16 15 11 10 6 5 4 3 2 0
Cop0
0 1 0 0 0 0
MFMC0
0 1 0 1 1
rt
rd
7
0 0 0 1 1
pos
31
1 1 1 1 1
sc
1
1
0
0 0
sel
1
0 0 1
6 5 5 5 5 1 2 3

Fig. 12

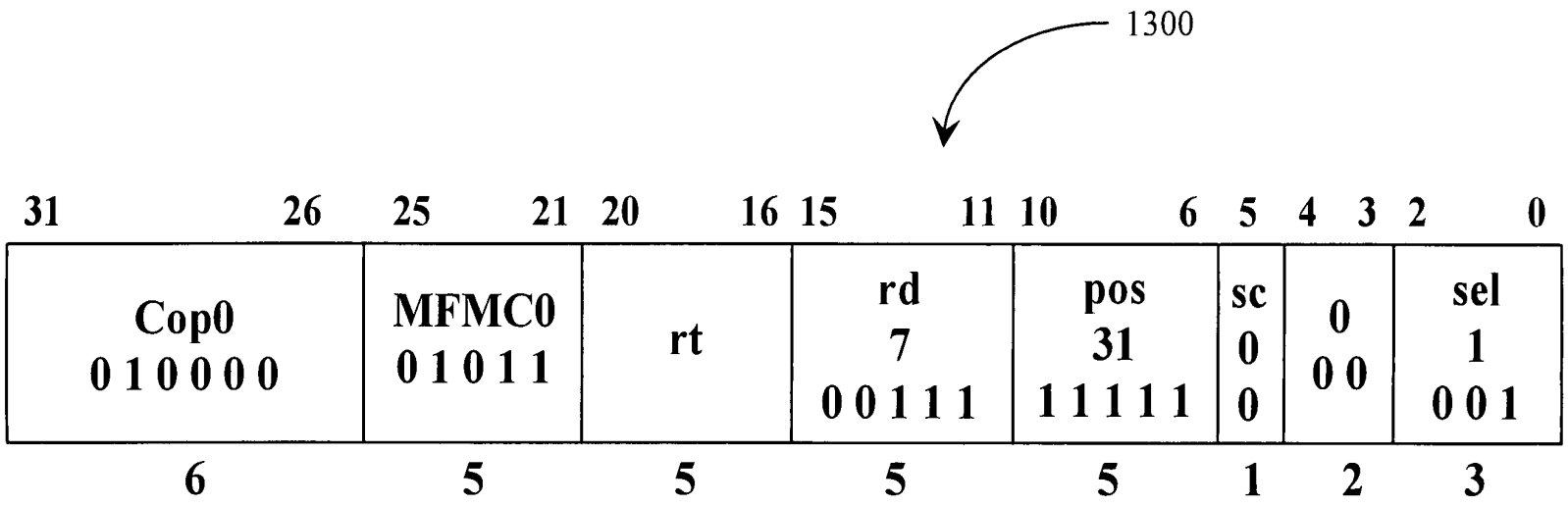

1300
31 26 25 21 20 16 15 11 10 6 5 4 3 2 0
Cop0
0 1 0 0 0 0
MFMC0
0 1 0 1 1
rt
rd
7
0 0 1 1 1
pos
31
1 1 1 1 1
sc
0
0
0
0 0
sel
1
0 0 1
6 5 5 5 5 1 2 3

Fig. 13

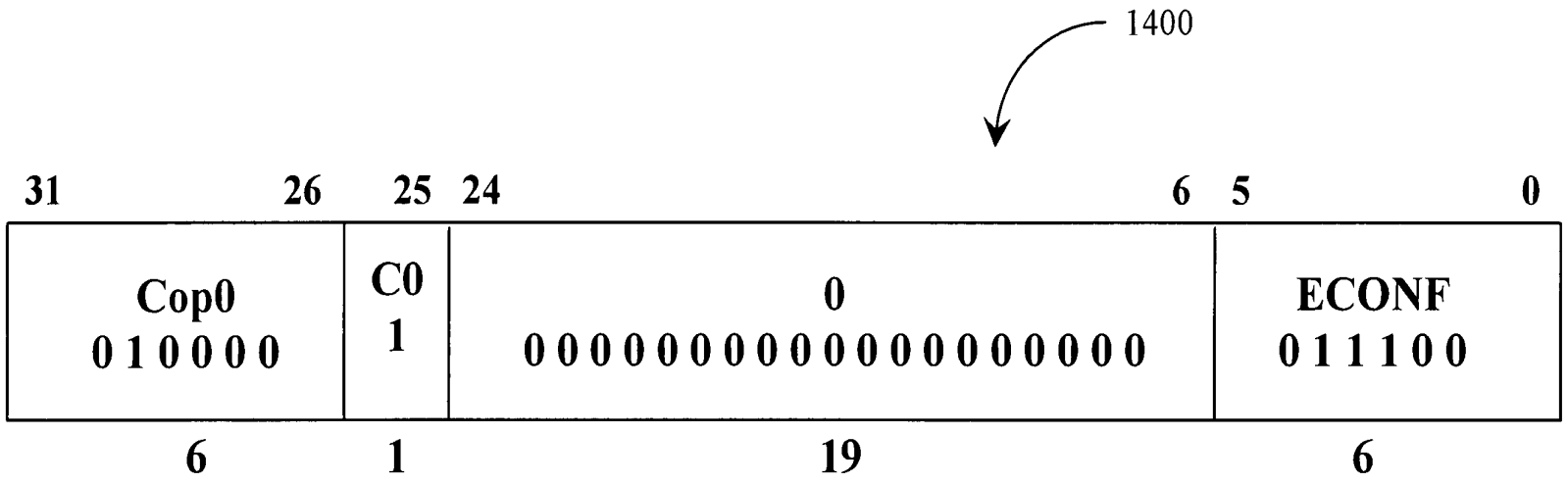

1400
31
26
25
24
6
5
0
Cop0
0 1 0 0 0 0
C0
1
0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
ECONF
0 1 1 1 0 0
6
1
19
6

Fig. 14

Register Name	New or Modified	CP0 Register Number	Register Select Number	Description
ThreadContext	New	4	1	Per Thread Read/Write Storage for OS use
ThreadConfig	New	6	1	Per-VPE register containing relatively non-volatile thread configuration data
ThreadSchedule	New	6	2	Optional per-thread register to assign issue bandwidth within VPE
VPESchedule	New	6	3	Optional per-VPE register to assign issue bandwidth within a processor
ThreadControl	New	7	1	Per-VPE register containing relatively volatile thread configuration data
ThreadStatus	New	12	4	Per-thread status information, includes copies of thread-specific bits of Status and EntryHi registers
Config4	New	16	4	Per-processor configuration information on thread and VPE-related resources
Status	Modified	12	0	Additions to CU3-CU1 semantics
Cause	Modified	13	0	New cause code
EntryLo	Modified	2,3	0	Previously reserved cache attribute assigned
Config3	Modified	16	3	Fields added to describe thread-related resource config.
EBase	Modified	15	1	Previously reserved bit used to inhibit VPE with corresponding CPUNum value
SRSCtl	Modified	12	2	Previously hard-wired field now Soft and a function the ThreadConfig register

1500

Fig. 15

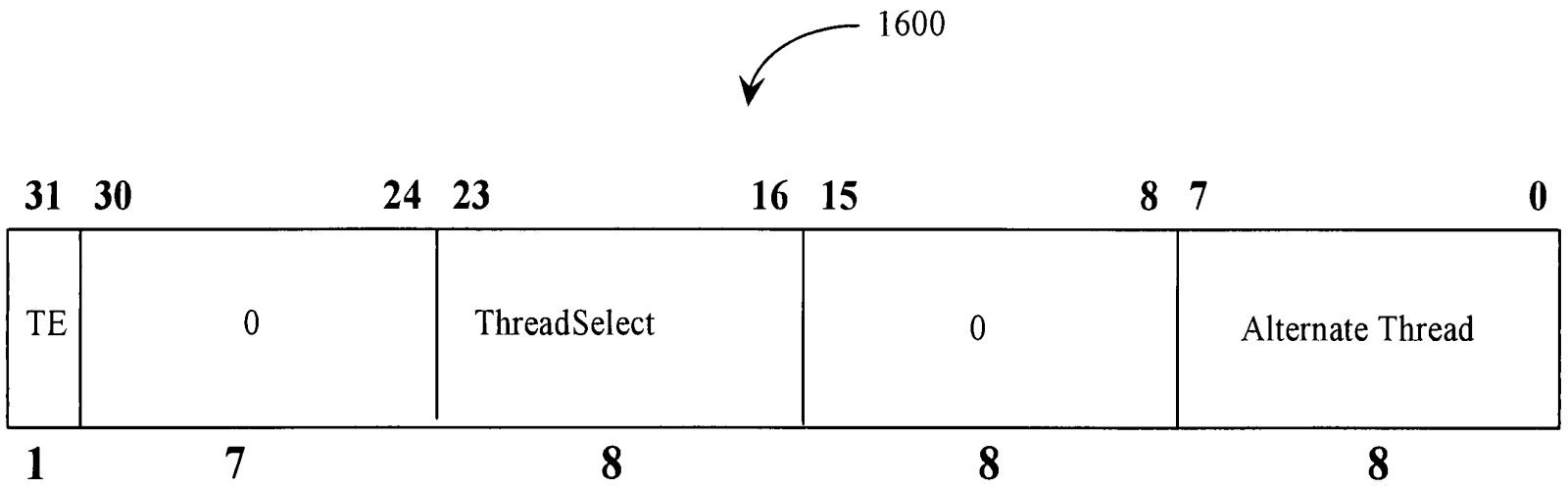
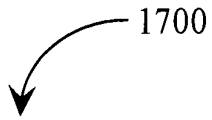

1600
31
30
24
23
16
15
8
7
0
TE
0
ThreadSelect
0
Alternate Thread
1
7
8
8
8

Fig. 16



Fields		Description	Read/Write	Reset State
Name	Bits			
TE	31	Threads enabled. Set by EMT instruction, cleared by DMT instruction. If set, multiple thread contexts may be simultaneously active. If cleared, only one thread may execute on the VPE.	R	0
ThreadSelect	16:23	Indicates the number (index) of the thread context of the thread issueing the MFCO instruction inspecting the register.	R	Max Thread Index
Alternate Thread	7:0	Thread index to be used on MTTR and MFTR instructions.	R/W	Undefined
0	31:24, 15:8	Must be written as 0. Return 0 on read.	0	0

Fig. 17

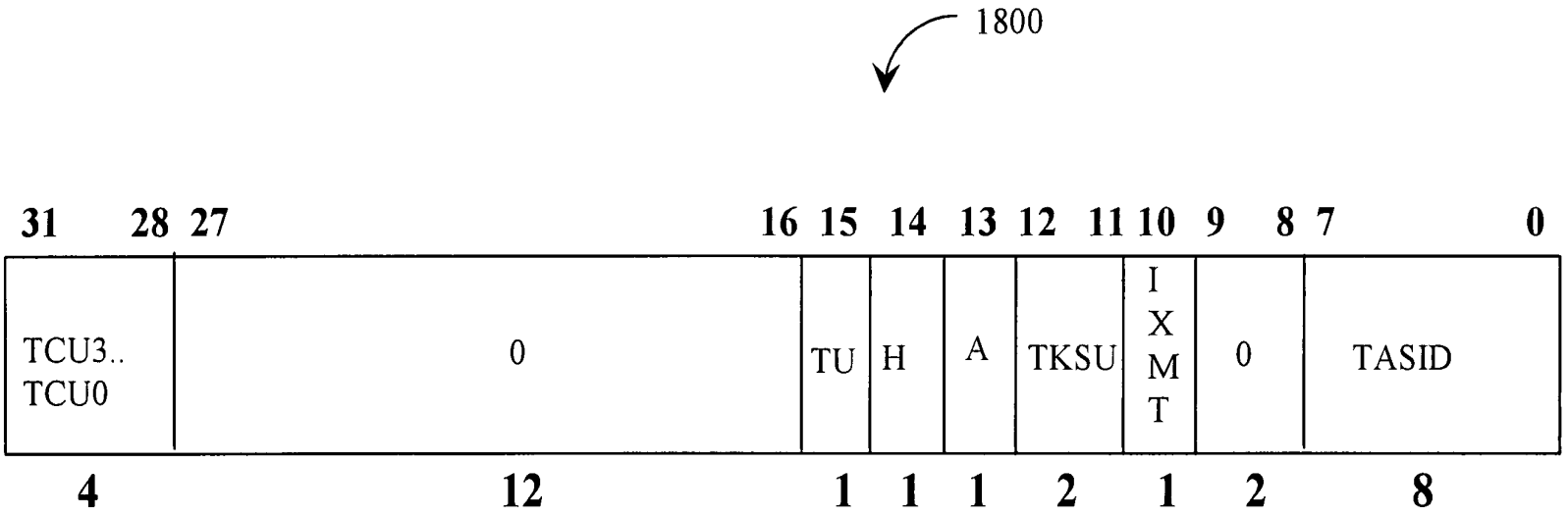

1800
31
28
27
16
15
14
13
12
11
10
9
8
7
0
TCU3..
TCU0
0
TU
H
A
TKSU
I
X
M
T
0
TASID
4
12
1
1
1
2
1
2
8

Fig. 18

Fields		Description	Read/ Write	Reset State	Fork State
Name	Bits				
TCU (TCU3.. TCU0)	31..28	Controls access and binding of threads to coprocessors 3, 2, 1, and 0 respectively. Status CU3..CU0 are identical to ThreadStatus TCU3..TCU0 of the thread refrencing status. The modification of either must bevisible in both.	R/W	0	0
TU	15	Thread underflow indication. Set by hardware in conjunction with a Thread Exception being raised in the case of a YIELD instruction that would deallocate the last allocated thread on a VPE. Cleared by any other Thread Exception.	R/W	0	0
H	14	Thread halted. When set, the associated thread has been halted and cannot be allocated, activated or scheduled.	R/W	0	0
A	13	Thread activated. Set automatically when a FORK instructioin allocates the thread context, and cleared automatically when a YIELD $0 instruction deallocated it.	R/W	#1	1
TKSU	12..11	Defined as per the Status register KSU field. This is the per-thread Kernel/ Supervisor/User state. Status.KSU is identical to ThreadStatus. TKSU of the thread referencing status. The modification of either must be visible in both.	R/W	#2	#3
IXMT	10	Interrupt Exempt. If set, thread will not take asynchronous exceptions such as interrupts.	R/W	0	0
TASID	7:0	Defined as per the EntryHi register ASID field. This is the per thread ASID value. EntryHi.ASID is identical to ThreadStatus.TASID of the thread referencing EntryHi. The modification of either must be visible in both.	R/W	#2	#3
0	31:16 10:8	Must be written as 0. Return 0 on read.	0	0	0

#1 - 1 for default/reset thread, 0 for all others
#2 - undefined

1900

#3 - copied from forking thread

Fig. 19

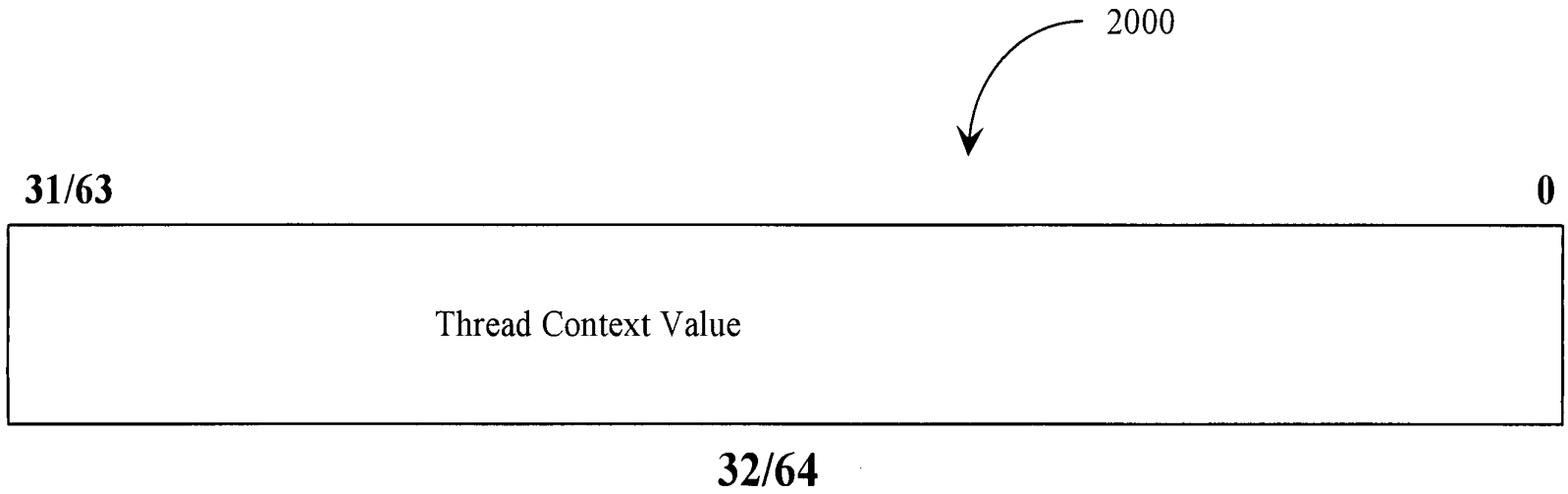


Fig. 20

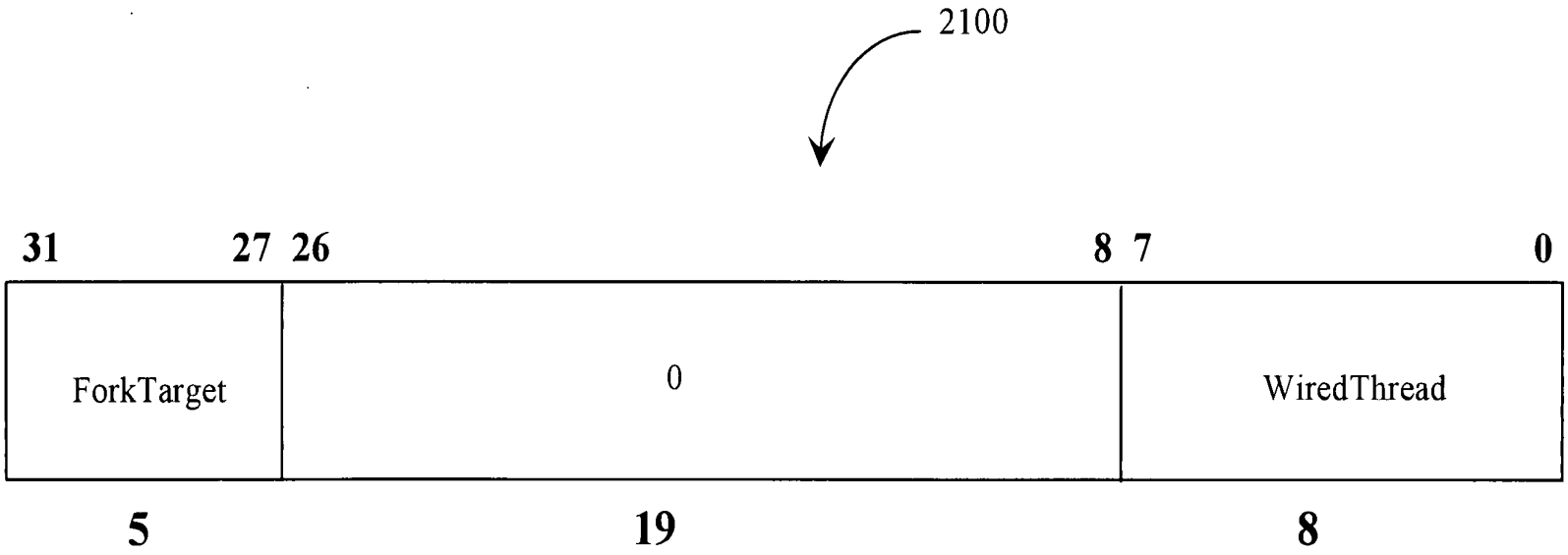
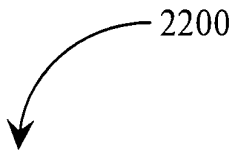


Fig. 21



Fields		Description	Read/ Write	Reset State
Name	Bits			
ForkTarget	31..27	GPR number to be used as destination of rt register value on a FORK instruction.	R or R/W	Preset or undefined
WiredThread	7:0	Index of the lowest numbered thread available for dynamic allocation	R/W	Undefined
0	26..8	Must be written as 0; return 0 on read.	0	0

Fig. 22

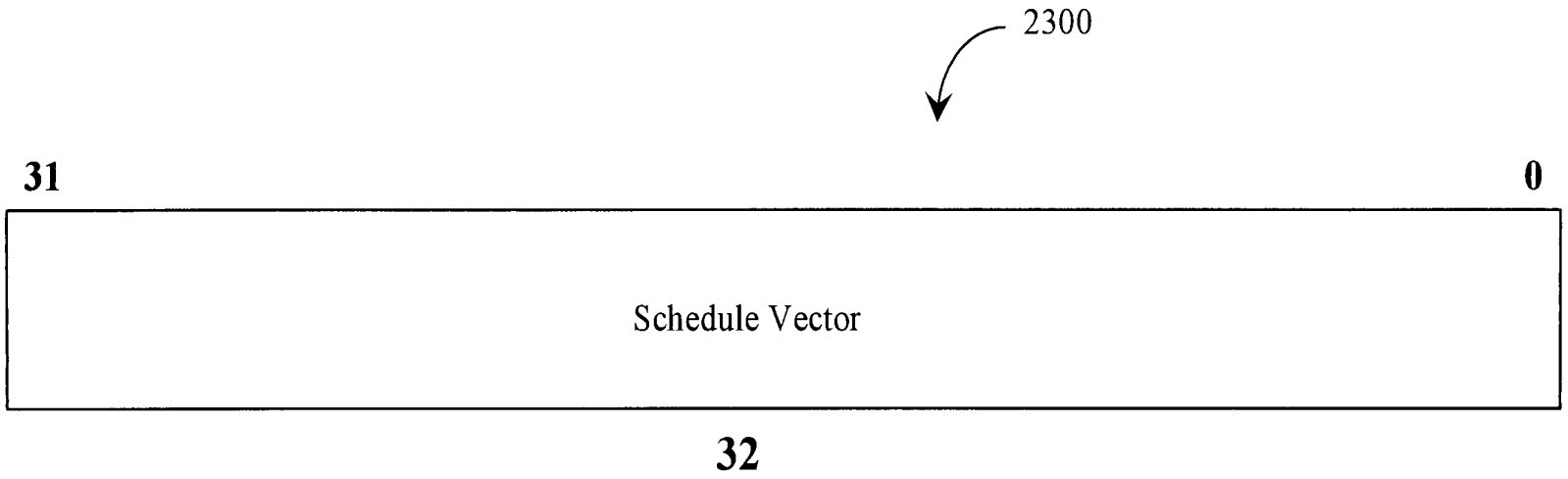


Fig. 23

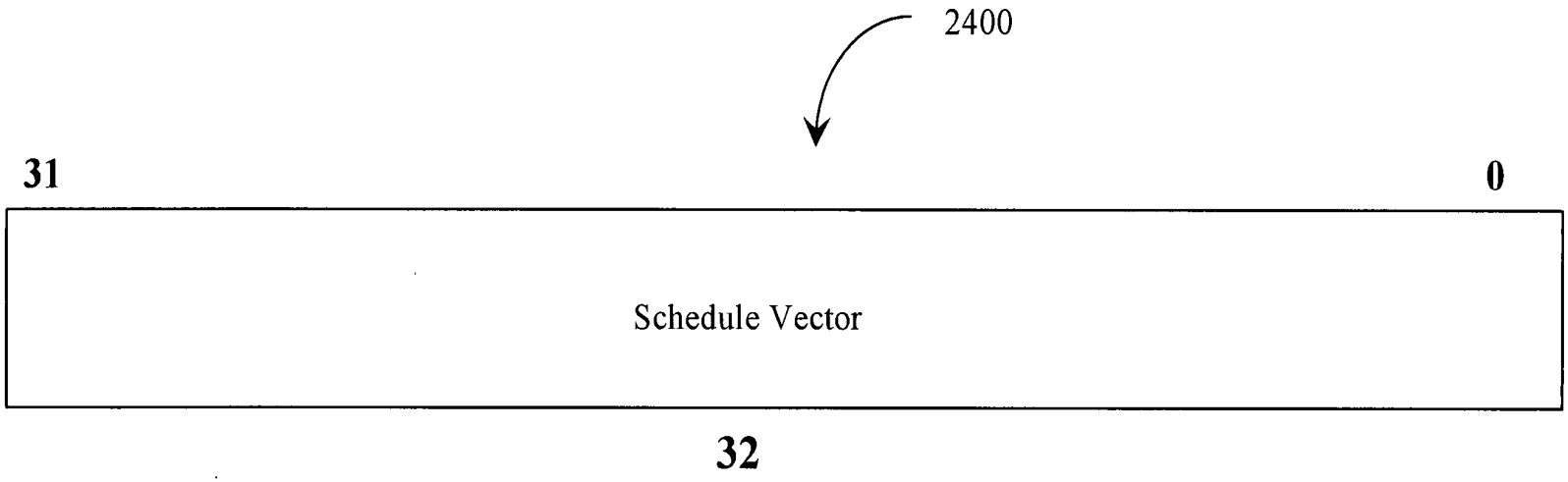


Fig. 24

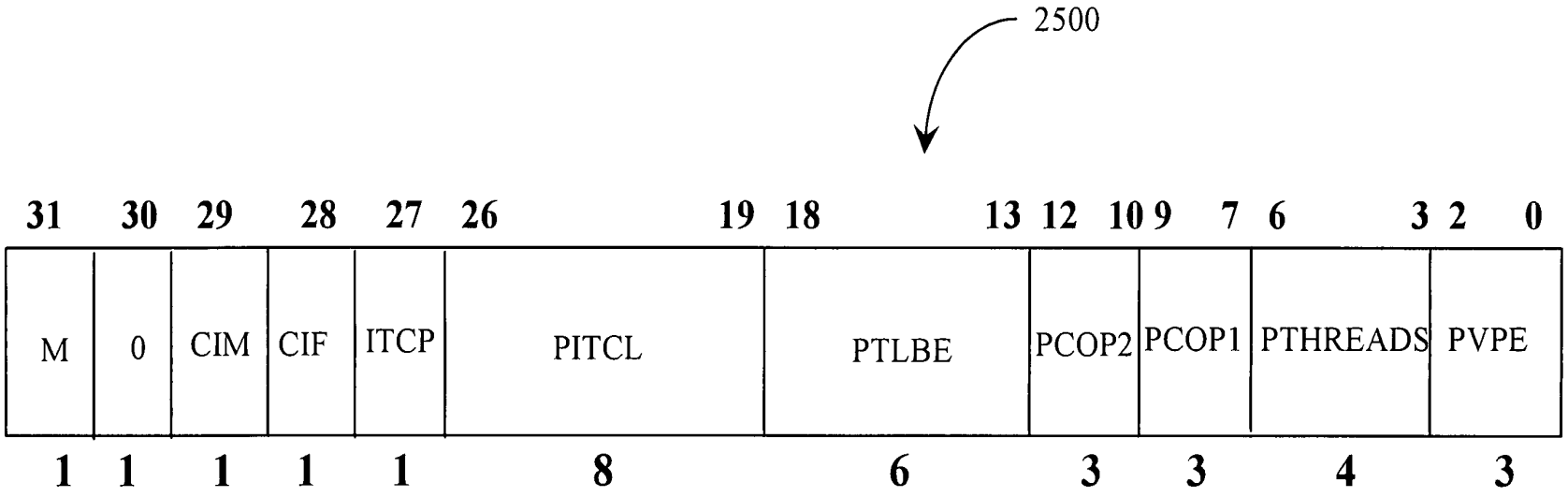
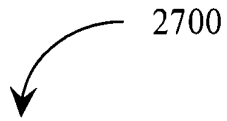

2500
31
30
29
28
27
26
19
18
13
12
10
9
7
6
3
2
0
M
0
CIM
CIF
ITCP
PITCL
PTLBE
PCOP2
PCOP1
PTHREADS
PVPE
1
1
1
1
1
8
6
3
3
4
3

Fig. 25

2600

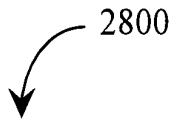
Fields		Description	Read/ Write	Reset State
Name	Bits			
M	31	This bit is reserved to indicate that a Config5 register is present	R	Preset
0	30	Reserved. Reads as 0. Must be written as o.	R	Preset
C1M	29	Allocatable CP1 coprocessors are media-extension capabl.	R	Preset
C1F	28	Allocatable CP1 coprocessors are floating-point capable.	R	Preset
ITCP	27	If set, ITC locations per page is configuarable. Otherwise Config3.NITC_PLocs is fixed.	R	Preset
PITCL	26:19	Log2 of total processor compliment of ITC storage locations	R	Preset
PTLBE	18:13	Log2 of total procesor compliment of TLB entry pairs	R	Preset
PCOP2	12:10	Log2 of total processor compliment of integrated and allocatable Coprocessor 2's	R	Preset
PCOP1	9:7	Log2 of total processor compliment of integrated and allocatable FP/MDMX Coprocessors.	R	Preset
PThreads	6:3	Log2 of total processor compliment of Thread contexts	R	Preset
PVPE	2:0	Log2 of total processor compliment of VPE contexts		

Fig. 26



Exception Code Value		Mnemonic	Description
Decimal	Hexadecimal		
25	16#19	Thread	Thread Allocation or De-allocation Error

Fig. 27



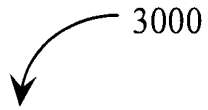
C(5:3) Value	Cache Coferency Attribute
7	References to page resolved through ITC storage rather than the cache hierarchy.

Fig. 28

Fields		Description	Read/ Write	Reset State
Name	Bits			
NITC_PLocs	30:28	Number of ITC Synchronization Locations per page of ITC Storage, encoded as Log2 of the number of locations per page.	R	Preset
		2#000 = 1		
		2#001 = 2		
		2#010 = 4		
		2#011 = 8		
		2#100 = 16		
		2#101 = 32		
		2#110 = 64		
		2#111 = 127		
NITC_Pages	27:16	Number of ITC Pages Available to VPE	R	Preset
NThreads	15:8	Number of thread contexts available minus 1. If 0, no multithreading capability is implemented.	R	Preset
VPC	3	Indicates that processor is in a VPE Configuration State. Settable by software only if the MVP bit is set.	R/RW	0
MVP	2	Indicates that the processor has multiple VPE contexts that may be configured. If MVP is set, the adjacent VPC bit may be written by software to enable VPE configuration. MVP may be cleared by software while VPC is set, such that a subsequent ECONF instruction will latch the zero value and prevent futher configuration until the next hard reset.	R/RW	Preset

Fig. 29

2900



Fields		Description	Read/ Write	Reset State
Name	Bits			
VPI	30	Virtual Processor Inhibit, if set, the virtual processor associated with the CPUNum value is inhibited from execution. If clear, VPE is started on ECONF. Thus the zero value necessary for direct software use as a base register is preserved for active VPE's.	R	Preset

Fig. 30

Address Bits 4:3 Value	ITC Storage Behavior	
2#00	Empty/Full Synchronized Storage Loads wiil cause the issueing thread to block if location is Empty, and reset the Empty state on returning a load value. Stores will cause the issueing thread to block if the location is Ful, and reset the full state on the location accepting a store value.	
2#01	Force Empty/Full Loads/Stores do not block. Loads set Empty state. Stores set Full state, regardless of previous value. Load value returned is that of last value to the location (or unpredictable if never initialized).	
2#10	Bypass Empty/Full Loads/Stores do not block, and do not affect Empty/Full.	
2#11	Status Control Informaton	
	Data Bit(s)	Meaning
	0	If set, location is empty, and will block on attempt to store as synchronized storage
	1	If set, location is Full and will block on an attempt to store as synchronized storage.
	2	Load-Blocked Thread indication. Value of 1 if a load has blocked on the location since the last setting of the Empty bit; 0 otherwise.
	3	Store-blocked Thread indication. Value of 1 if a store has bl;ocked on the location since the last setting of the Full bit, 0 otherwise.
	63..4	Implementation Dependent State.

3100

Fig. 31

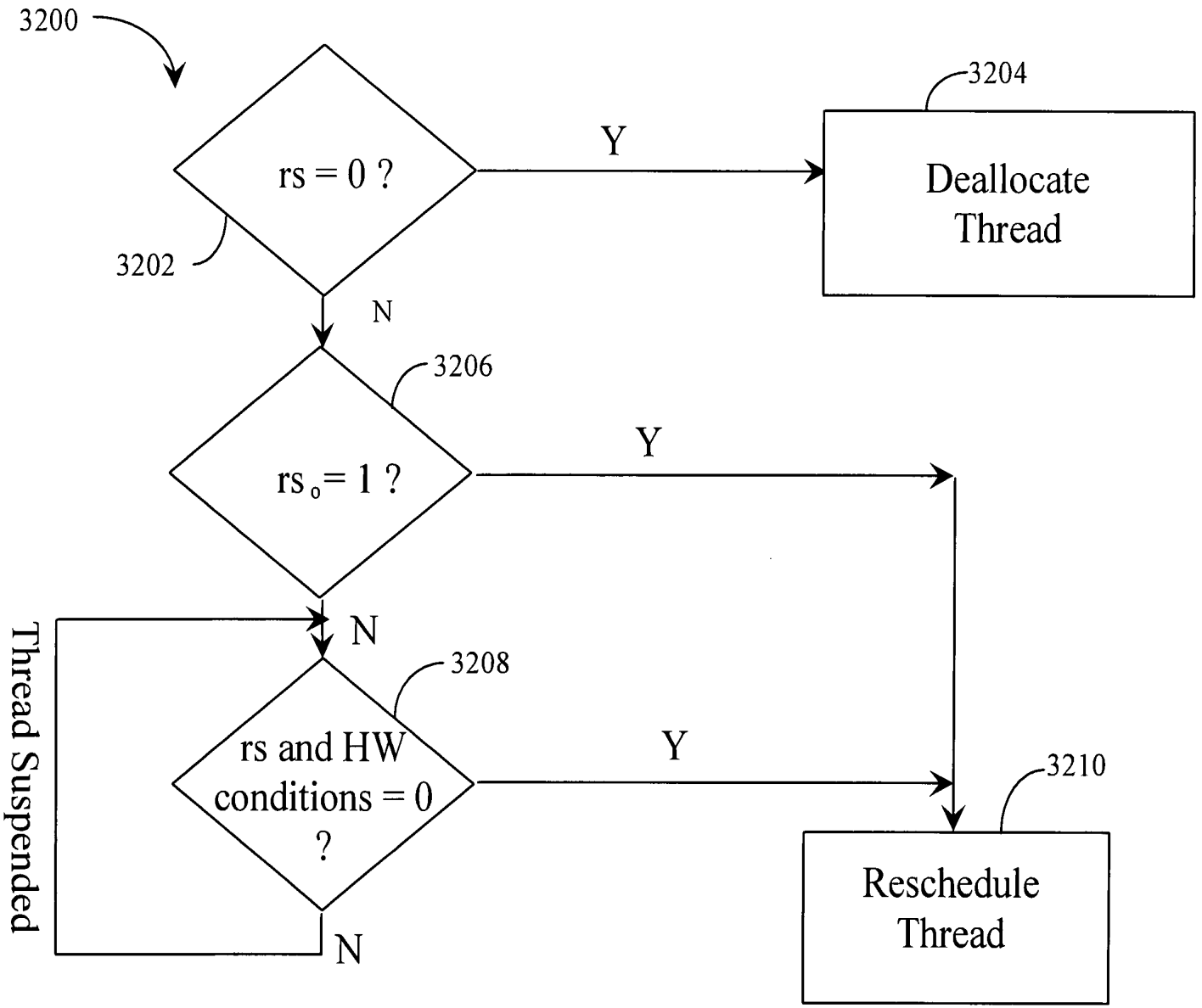

3200
rs = 0 ?
3202
Y
3204
Deallocate Thread
N
3206
rs$_0$ = 1 ?
Y
N
3208
rs and HW conditions = 0 ?
Y
3210
Reschedule Thread
N
Thread Suspended

Fig. 32

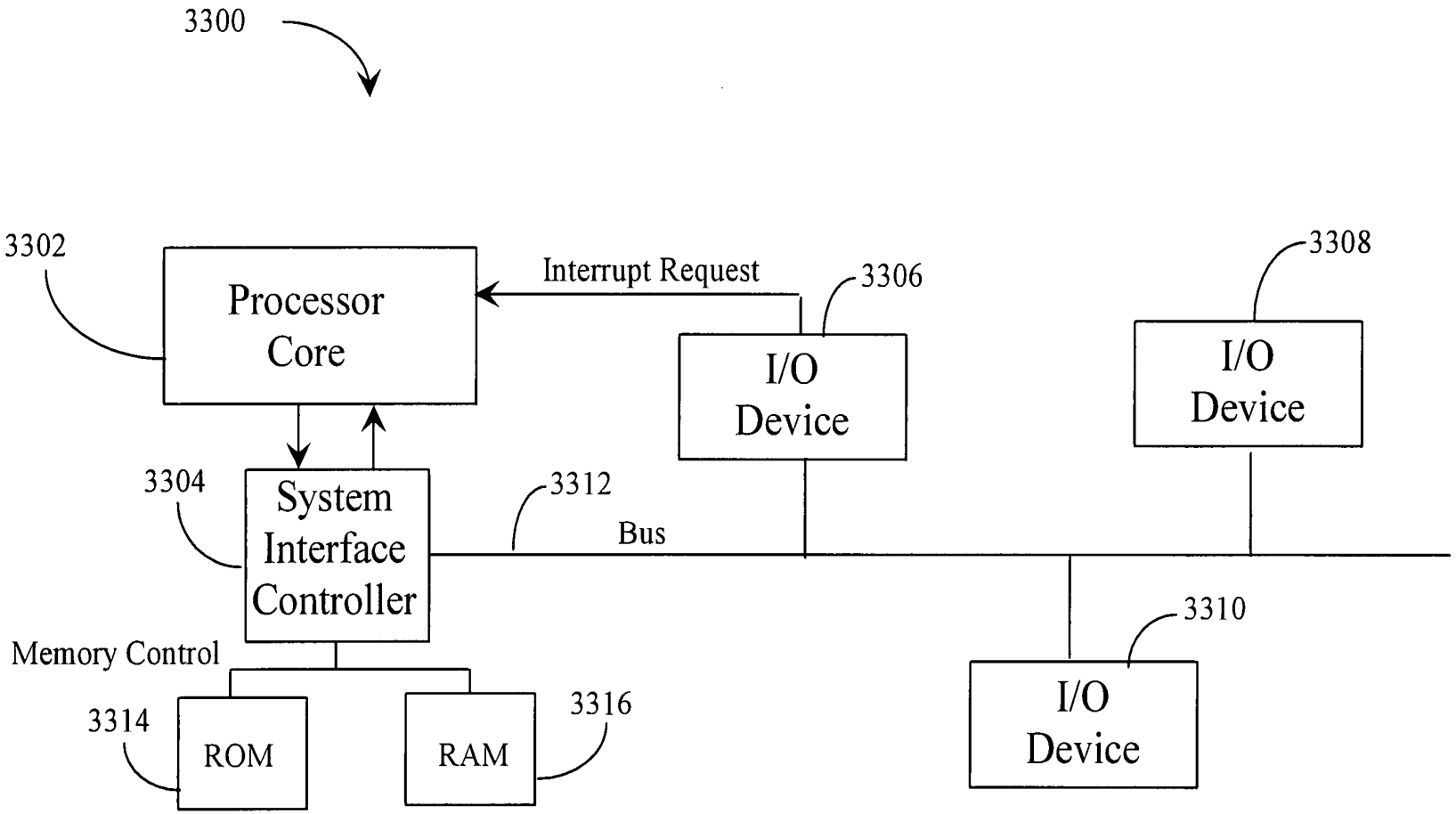

3300
3302
Processor Core
Interrupt Request
3306
I/O Device
3308
I/O Device
3304
System Interface Controller
3312
Bus
Memory Control
3314
ROM
RAM
3316
3310
I/O Device

Fig. 33

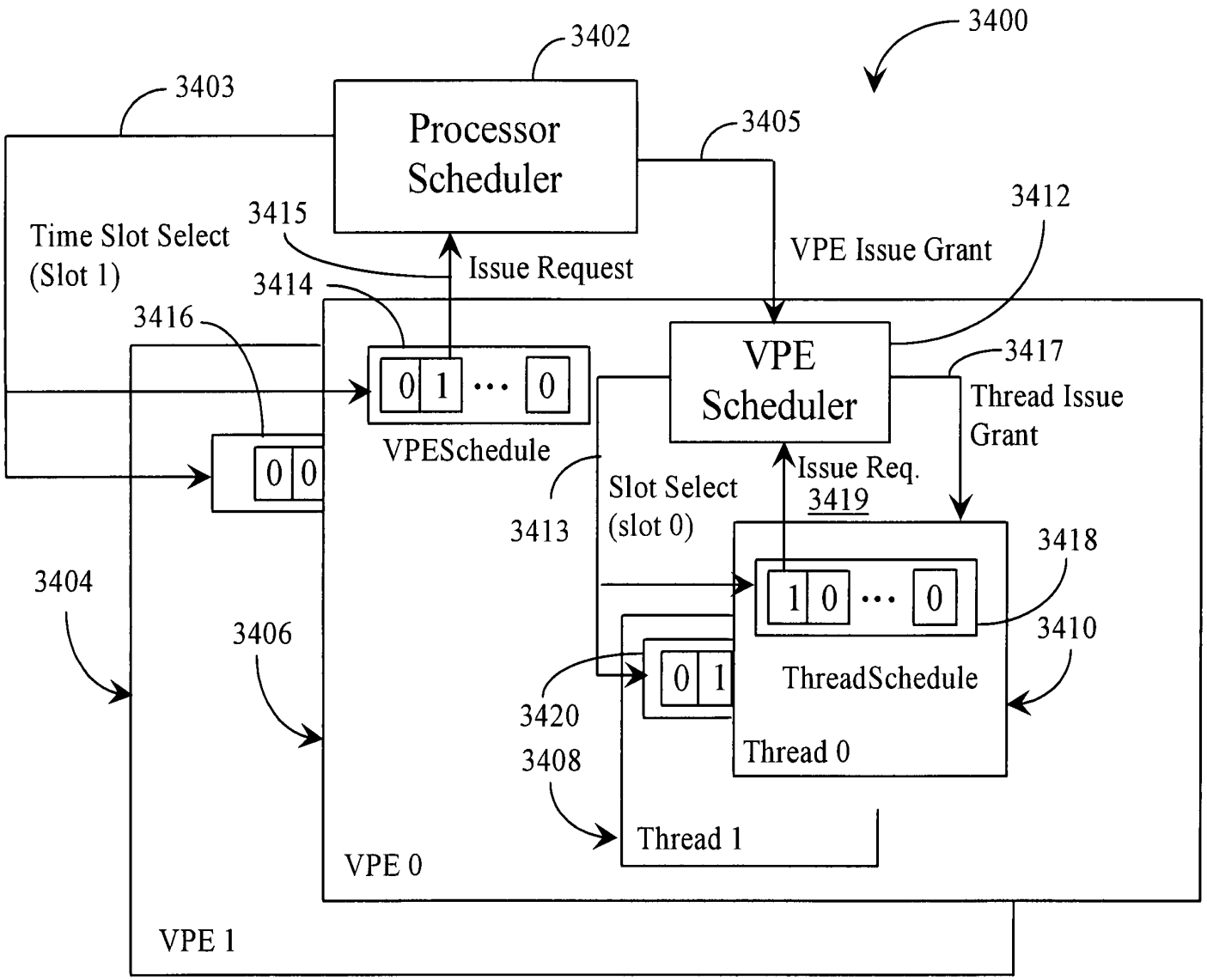

3400
3402
3403
Processor Scheduler
3405
3412
3415
Time Slot Select (Slot 1)
Issue Request
VPE Issue Grant
3414
3416
VPE Scheduler
3417
Thread Issue Grant
0 1 ... 0
VPESchedule
0 0
Issue Req. 3419
3413
Slot Select (slot 0)
3418
3404
1 0 ... 0
3406
3410
0 1
ThreadSchedule
3420
Thread 0
3408
Thread 1
VPE 0
VPE 1

Fig. 34